Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-8. (canceled)

9. (currently amended) ~~The method of claim 1 with additional steps of:~~ A method of providing thermal stress relieve for packages used for mounting semiconductor devices, comprising steps of:

providing a circuit board having at least one point of electrical contact;

forming one or more layers of thermal stress relieve material on said circuit board;

providing one or more semiconductor devices for mounting on said circuit board, said one or more semiconductor devices having been provided with points of electrical contact; and

establishing electrical contact between said at least one point of electrical contact provided on said circuit board and said points of electrical contact provided in said semiconductor devices, said establishing electrical contact between said at least one point of electrical contact provided on said circuit board and said points of electrical contact provided in said semiconductor devices comprising Printed Circuit Board technology or Build Up Board technology, said Printed Circuit Board technology comprising:

(i) creating one or more openings in said created layers of thermal stress relieve material whereby said one or more openings align with one or more overlying points of electrical contact on one or more created layers of said thermal stress relieve material;

(ii) depositing a layer of conductive material over said created layers of thermal stress relieve material, including said openings;

(iii) patterning said layer of conductive material, forming a upper layer of interconnect lines and contact pads on said created one or more layers of said thermal stress relieve material, exposing the surface of said thermal stress relieve material;

depositing a layer of dielectric over said upper layer of interconnect lines, including said exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric, exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said at least one point of electrical contact provided on said circuit board, said conductive pads further being points of electrical contact for said one or more semiconductor devices.

10. (previously presented) The method of claim 9 with additional steps of:

positioning said semiconductor devices above said circuit board, said array of conductive pads in the layer of dielectric being aligned and in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by thermal reflow.

11. (currently amended) The method of claim ~~1~~ 9 wherein said Build Up Board technology comprises interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact

pads being created on an underlying or first layer of thermal stress relieve material, comprising steps of:

depositing a first layer of conductive material on a first layer of thermal stress relieve material;

patterning said first layer of conductive material, creating a first pattern of interconnect lines or contact pads;

creating a second layer of thermal stress relieve material on said first layer of thermal stress relieve material including said first pattern of interconnect lines or contact pads;

creating vias in said second layer of stress relieve material, said vias overlying interconnect lines or contact pads of said first pattern;

depositing a second layer of conductive material on said second layer of stress relieve material, including said vias, connecting said second layer of conductive material to said first pattern of interconnect lines or contact pads; and

patterning said second layer of conductive material, creating a second pattern of interconnect lines or contact pads, exposing said created second layer of thermal stress relieve material.

12. (original) The method of claim 11 wherein said creation of vias comprises methods of lithographic etching or laser drilling.

13. (previously presented) The method of claim 11, said Build Up Board technology being applied one or more times during said step of creating a layer of thermal stress relieve material on said circuit board, creating multiple overlying vias interconnecting multiple layers of interconnect lines and contact pads.

14. (previously presented) The method of claim 11 wherein said depositing a first layer of conductive material comprises steps of electroless seeding followed by electroplating of said first layer of said thermal stress relieve material.

15. (previously presented) The method of claim 11 wherein said depositing a second layer of conductive material comprises steps of electroless seeding followed by electroplating of said created second layer of said thermal stress relieve material, said step of electroless seeding followed by electroplating being performed after said creation of vias in said second layer of thermal stress relieve material.

16. (previously presented) The method of claim 11 with additional steps of:

depositing a layer of dielectric over said second layer of conductive material, including said exposed second layer of thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric, exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on said circuit board, said conductive pads further being points of electrical contact for said one or more semiconductor devices.

17. (previously presented) The method of claim 16 with additional steps of:

positioning said semiconductor devices above said circuit board, said array of conductive pads of said second pattern of interconnect lines or contact pads being aligned and in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads of said second pattern of interconnect lines or contact pads with said points of electrical contact for said semiconductor devices by thermal reflow.

18. (currently amended) The method of claim ~~1~~ 9 with an additional step of etching or swelling one or more of said created layers of thermal stress relieve material, thereby roughening said created layers, enhancing adhesion for a subsequent electroless metal deposition, said additional step being performed after said step of creating a layer of thermal stress relieve material.

19. (currently amended) The method of claim ~~1~~ 9 with an additional step of curing one or more of said created layers of thermal stress relieve material, said additional step being performed after said step of creating a layer of thermal stress relieve material.

20. (previously presented) The method of claim 19 wherein said curing comprises thermal curing technology.

21. (previously presented) The method of claim 19 wherein said curing comprises E-beam curing technology.

22. (previously presented) The method of claim 19 wherein said curing comprises UV curing technology.

23. (currently amended) The method of claim ~~1~~ 9 wherein establishing electrical contact between said at least one point of electrical contact provided on said circuit board and said points of

electrical contact provided in said semiconductor devices is providing contact pads on said created layers of thermal stress relieve material, said contact pads having been connected to at least one of said points of electrical contact provided on said circuit board, said contact pads further being points of electrical contact for said semiconductor devices.

24. (currently amended) The method of claim ~~1~~ 9 wherein establishing electrical contact between said at least one point of electrical contact provided on said circuit board and said points of electrical contact provided in said semiconductor devices is providing at least one conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact provided on said circuit board using PCB technology or Build Up Board technology, said conducting interconnects further being points of electrical contact for said semiconductor devices.

25. (currently amended) The method of claim ~~1~~ 9 wherein establishing electrical contact between said at least one point of electrical contact provided on said circuit board and said points of electrical contact provided in said semiconductor devices is providing at least one contact pad on said layers of thermal stress relieve material in addition to providing at least one conducting interconnect through said layers of thermal stress relieve material, said contact pads on said layers of thermal stress relieve material having been connected to at least one of said conducting interconnect through said layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact points provided on said circuit board using PCB technology or Build Up Board technology, said contact pads on said

layers of thermal stress relieve material being points of electrical contact for said semiconductor devices.

26. (previously presented) The method of claim 25 wherein providing at least one contact pad on said created layers of thermal stress relieve material comprises steps of:

depositing a layer of conducting material over said created layer of thermal stress relieve material;

patterning said layer of conducting material, creating a pattern of interconnect lines on said created layer of thermal stress relieve material, exposing said thermal stress relieve material;

depositing a layer of dielectric over said pattern of interconnect lines, including said exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric, exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

27. (previously presented) The method of claim 26 with additional steps of:

positioning said semiconductor devices above said circuit board, said array of conductive pads in the layer of dielectric being aligned and in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by thermal reflow.

28. (currently amended) The method of claim ~~1~~ 9 wherein said Build Up Board technology is interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads being created on a BGA surface, comprising steps of:

providing a semiconductor surface having been provided with points of electrical contact;

creating a layer of thermal stress relieve material on said semiconductor surface;

creating vias in said layer of stress relieve material, said vias overlying said points of electrical contact provided in said semiconductor surface;

depositing a layer of conductive material on said layer of stress relieve material, including said vias, connecting said layer of conductive material to points of electrical contact provided in said semiconductor surface; and

patterning said layer of conductive material, creating a pattern of interconnect lines or contact pads, exposing said created layer of thermal stress relieve material.

29. (previously presented) The method of claim 28 wherein said semiconductor surface is the surface of a BGA substrate.

30. (previously presented) The method of claim 28 wherein said creation of vias comprises methods of lithographic etching or laser drilling.

31. (previously presented) The method of claim 28 wherein said Build Up Board technology is applied one time during said step of creating a layer of thermal stress relieve material on said semiconductor surface, creating a first layer of thermal stress relieve material on said semiconductor surface.

32. (previously presented) The method of claim 28 wherein said depositing a layer of conductive material comprises steps of electroless seeding followed by electroplating of said underlying layer of said thermal stress relieve material, said steps of electroless seeding followed by electroplating being performed after said creation of vias in said created layer of thermal stress relieve material.

33. (previously presented) The method of claim 28 with additional steps of:

depositing a layer of dielectric over said pattered layer of conductive material, including said exposed thermal stress relieve material;

depositing a solder mask over said layer of dielectric; and

patterning said layer of dielectric, exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

34. (previously presented) The method of claim 33 with additional steps of:

positioning said semiconductor devices above said circuit board, said array of conductive pads in the layer of dielectric being aligned and in contact with said points of electrical contact of said semiconductor devices; and

connecting said array of conductive pads in the layer of dielectric with said points of electrical contact for said semiconductor devices by thermal reflow.

35-42. (canceled).

43. (currently amended) ~~The structure of claim 35, additionally comprising:~~ A structure for providing thermal stress relieve for packages that are used for the mounting of semiconductor devices, comprising:

a circuit board on which at least one point of electrical contact has been provided;

one or more layers of thermal stress relieve material created on said circuit board;

one or more semiconductor devices for mounting on said circuit board, said semiconductor devices having been provided with points of electrical contact; and

electrical contact between said point of electrical contact provided on said circuit board and said points of electrical contact provided in said semiconductor devices, said electrical contact having been established using Printed Circuit Board technology or Build Up Board technology, said Printer Board technology comprising creating one or more openings in said one or more layers of thermal stress relieve material aligned with said at least one point of electrical contact provided on said circuit board, by depositing a layer of conductive material over said created layers of thermal stress relieve material, including said one or more openings and by creating an upper layer of interconnect lines and contact pads formed by patterning said layer of conductive material on said layer of said thermal stress relieve material;

a layer of dielectric deposited over said upper layer of interconnect lines, including said exposed thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

44. (previously presented) The structure of claim 43, additionally comprising:

said semiconductor devices having been positioned above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

said array of conductive pads in the layer of dielectric having been connected with said points of electrical contact for said semiconductor devices.

45. (currently amended) The structure of claim ~~35~~ 43 wherein said Build Up Board technology comprises interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads having being created on a first layer of thermal stress relieve material, said second pattern of interconnect lines and contact pads having been created on a second layer of thermal stress relieve material.

46. (canceled).

47. (previously presented) The structure of claim 45, said Build Up Board technology having been applied one or more times during creating a layer of thermal stress relieve material on said circuit board, having created multiple overlying vias interconnecting multiple layers of interconnect lines and contact pads.

48. (canceled).

49. (canceled).

50. (previously presented) The structure of claim 45, additionally comprising:

a layer of dielectric deposited over said second layer of conductive material, including said second layer of thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric having been created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on said circuit board, said conductive pads further being points of electrical contact for said one or more semiconductor devices.

51. (previously presented) The structure of claim 50, additionally comprising:

said semiconductor devices having been positioned above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

said array of conductive pads in the layer of dielectric having been connected with said points of electrical contact for said semiconductor devices.

52. (currently amended) The structure of claim ~~35~~ 43 with additionally comprising etching or swelling one or more of said created layers of thermal stress relieve material, thereby having roughened said created layers and thereby enhancing adhesion for a subsequent electroless metal deposition.

53. (currently amended) The structure of claim ~~35~~ 43 with additionally said one or more layers of thermal stress relieve material having been cured.

54-56. (canceled).

57. (currently amended) The structure of claim ~~35~~43, electrical contact between said point of electrical contact provided in said circuit board and said points of electrical contact provided in said semiconductor devices having been established by providing contact pads on said created layers of thermal stress relieve material, said contact pads having been connected to at least one of said points of electrical contact provided on said circuit board, said contact pads further being points of electrical contact for said semiconductor devices.

58. (currently amended) The structure of claim ~~35~~43, electrical contact between said point of electrical contact provided in said circuit board and said points of electrical contact provided in said semiconductor devices having been established by providing at least one conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact provided on said circuit board using interconnect methods of PCB technology or Build Up Board technology, said conducting interconnects further being points of electrical contact for said semiconductor devices.

59. (currently amended) The structure of claim ~~35~~43, electrical contact between said point of electrical contact provided in said circuit board and said points of electrical contact provided in said semiconductor devices having been established by providing at least one contact pad on said created layers of thermal stress relieve material in addition to having provided at least one conducting interconnect through said created layers of thermal stress relieve material, said

contact pads on said created layers of thermal stress relieve material having been connected to said at least one conducting interconnect through said created layers of thermal stress relieve material, said conducting interconnects having been connected to at least one of said points of electrical contact points provided on said circuit board, said contact pads on said created layers of thermal stress relieve material being points of electrical contact for said semiconductor devices.

60. (previously presented) The structure of claim 59 wherein at least one contact pad on said created layers of thermal stress relieve material comprises:

a patterned layer of conducting material over said created layer of thermal stress relieve material, comprising a pattern of interconnect lines on said created layer of thermal stress relieve material;

a layer of dielectric deposited over said pattern of interconnect lines;

a solder mask deposited over said layer of dielectric; and

said layer of dielectric having been patterned, exposing an array of conductive pads in the layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

61. (previously presented) The structure of claim 60, additionally comprising:

said semiconductor devices having been positioned above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

said array of conductive pads in the layer of dielectric having been connected with said points of electrical contact for said semiconductor devices.

62. (currently amended) The structure of claim ~~39~~ 43 wherein said Build Up Board technology comprises interconnecting a first pattern of interconnect lines and contact pads to a second pattern of interconnect lines and contact pads, said first pattern of interconnect lines and contact pads being created on a BGA surface, comprising:

a semiconductor surface having been provided with points of electrical contact in its surface;

a layer of thermal stress relieve material having been created on said semiconductor surface;

vias having been created in said layer of stress relieve material, said vias overlying said points of electrical contact provided in said semiconductor surface;

a layer of conductive material having been deposited on said layer of stress relieve material, including said vias, connecting said layer of conductive material to electrical contact provided in said semiconductor surface; and

said layer of conductive material having been patterned, having created a pattern of interconnect lines or contact pads, exposing said created layer of thermal stress relieve material.

63. (original) The structure of claim 62 wherein said semiconductor surface is the surface of a BGA substrate.

64. (canceled).

65. (previously presented) The structure of claim 62, said Build Up Board technology having been applied one time during said step of creating a layer of thermal stress relieve material on

said semiconductor surface, having created a first created layer of thermal stress relieve material on said semiconductor surface.

66. (canceled).

67. (previously presented) The structure of claim 62, additionally comprising:

a layer of dielectric deposited over said pattered layer of conductive material, including said exposed thermal stress relieve material;

a solder mask deposited over said layer of dielectric; and

an array of conductive pads in the layer of dielectric created by patterning said layer of dielectric, said conductive pads having been connected to at least one of said points of electrical contact provided on said circuit board, said conductive pads further being points of electrical contact for said semiconductor devices.

68. (previously presented) The structure of claim 67, additionally comprising:

said semiconductor devices having been positioned above said circuit board such that said array of conductive pads in the layer of dielectric aligns and is in contact with said points of electrical contact of said semiconductor devices; and

said array of conductive pads in the layer of dielectric having been connected with said points of electrical contact for said semiconductor devices.

69-73. (canceled).

74. (new) The method of claim 9, said semiconductor devices being flip chip devices having been provided with solder bumps.

75. (new) The method of claim 9 wherein said circuit board is a Printed Circuit Board.

76. (new) The method of claim 9 wherein said thermal stress relieve material comprises Elastomer or any other Thermal Compliant material.

77. (new) The method of claim 9 wherein said creating one or more openings in said created layers of thermal stress relieve material comprises methods of photolithography.

78. (new) The method of claim 9 wherein said depositing a layer of conductive material over said created layers of thermal stress relieve material comprises steps of electroless seeding followed by electroplating of said created layers of said thermal stress relieve material.

79. (new) The structure of claim 43, said semiconductor devices being flip chip devices having been provided with solder bumps.

80. (new) The structure of claim 43 wherein said circuit board is a Printed Circuit Board.

81. (new) The structure of claim 43 wherein said thermal stress relieve material comprises Elastomer or any other Thermal Compliant material.